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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/448,756	11/24/1999	JUN KOYMA	0756-2070	5419

22204 7590 01/29/2003

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EXAMINER
BELL, PAUL A

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 01/29/2003

#16

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/448,756	KOYMA ET AL.	
	Examiner	Art Unit	
	PAUL A BELL	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/427,096* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11, 15* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-38, are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. (See MPEP 608.04, 706.03(o), 2163.03)

In regards to claims 1,7, 13, 17, 19, 25, 31, and 35 the phrase "a crystalline semiconductor layer" can not be found in the original 4/21/1995 disclosure and claims. The examiner contends the specification on page 7 instead teaches "Amorphous Silicon" being used in the semiconductor layer.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

4. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the

application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsumoto (5,323,042).

With regard to claim 1 Matsumoto teaches an active matrix type display device comprising: a substrate having an insulating surface , a plurality of pixel electrodes arranged in a matrix form over said substrate , a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor, a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes (column 1, lines 5-12 figure 1, item 12, figure 4, item 6); and a driver circuit comprising a plurality of thin film transistors for driving said plurality of switching elements (figure 1, item 13, figure 4, item 2 and 3), wherein each of said plurality of thin film transistors comprises a crystalline semiconductor layer (column 3, lines 59-64), a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film (figure 1, items 26, 24, and 22).

With regard to claim 2 Matsumoto teaches wherein said gate electrode is located over said semiconductor layer (figure 1, items 26 and 11).

With regards to claim 3 Matsumoto teaches wherein all of said plurality of thin film transistors are p-type (column 5, line 67-68).

With regard to claim 4 Matsumoto teaches wherein all of said plurality of thin film transistors are n-type (column 5, line 67-68).

With regard to claim 5 Matsumoto teaches wherein said substrate is a glass substrate (column 3, line 3).

With regard to claim 6 Matsumoto teaches wherein said crystalline semiconductor layer comprises silicon (column 3, line 60).

With regard to claim 7 Matsumoto teaches an active matrix type display device comprising: a substrate having an insulating surface, a plurality of pixel electrodes arranged in a matrix form over said substrate, a plurality of switching elements operationally connected to said pixel electrodes, each of said switching elements comprising a thin film transistor, a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes (column 1, lines 5-12 figure 1, item 12, figure 4, items 6 and 7), and a driver circuit comprising a plurality of thin film transistors for driving said plurality of switching elements (figure 1, item 13, figure 4, item 2 and 3), wherein each of said plurality of thin film transistors comprises a crystalline semiconductor layer (column 3, lines 59-64), a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film (figure 1, items 26, 24, and 22) , wherein said crystalline semiconductor layer has source and drain regions and at least one lightly doped region (column 3, lines 7-17).

With regard to claim 8 Matsumoto teaches wherein said substrate is a glass substrate (column 3, line 3).

With regard to claim 9 Matsumoto teaches wherein said source and drain regions and said at least one lightly doped region are doped with phosphorus (column 4, lines 1-35).

With regard to claim 10 Matsumoto teaches wherein said source and drain regions and said at least one lightly doped region are doped with boron (column 4, lines 1-35).

With regard to claim 11 Matsumoto teaches wherein said gate electrode is located over said semiconductor layer (figure 1, items 26 and 11) .

With regard to claim 12 Matsumoto teaches wherein said crystalline semiconductor layer comprises silicon (column 3, line 60).

With regard to claim 13 Matsumoto teaches an active matrix type display device comprising: a substrate having an insulating surface; a plurality of pixel electrodes arranged in a matrix form over said substrate; a plurality of switching elements operationally connected to said pixel electrodes (column 1, lines 5-12 figure 1, item 12, figure 4, item 7), each of said switching elements comprising a thin film transistor (figure 1, item 12, figure 4, item 6), a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes (figure 4, item 6); and a CMOS circuit comprising at least one n-channel type thin film transistor and one p-channel type thin film transistor (column 2, line 68), wherein each of said n-channel and p-channel type thin film transistors comprises a crystalline semiconductor layer (column 3, lines 59-64), a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film (figure 1, items 26, 24, and 22).

With regard to claim 14 Matsumoto teaches wherein aid substrate is a glass substrate (column 3, line 3).

With regard to claim 15 Matsumoto teaches wherein said gate electrode is located over said semiconductor layer (figure 1, items 26 and 11) .

With regard to claim 16 Matsumoto teaches wherein said crystalline semiconductor layer comprises silicon (column 3, line 60).

With regard to claim 17 Matsumoto teaches an active matrix type display device comprising: a substrate having an insulating surface, a plurality of pixel electrodes arranged in a matrix form over said substrate, a plurality of switching elements operationally connected to said pixel electrodes (column 1, lines 5-12 figure 1, item 12, figure 4, item 6), each of said switching elements comprising a thin film transistor (figure 1, item 12, figure 4, item 6), a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes (figure 4, item 6), and a CMOS circuit comprising at least one n-channel type thin film transistor and one p-channel type thin film transistor (column 2, line 68), each of said thin film transistors comprising a crystalline semiconductor layer (column 3, lines 59-64), a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film (figure 1, items 26, 24, and 22), wherein said crystalline semiconductor layer has source and drain regions and at least one lightly doped region (column 3, lines 7-17).

With regard to claim 18 Matsumoto teaches wherein said substrate is a glass substrate (column 3, line 3).

With regard to claim 19 Matsumoto teaches an active matrix type display device comprising: a substrate having an insulating surface, a plurality of pixel electrodes arranged in a matrix form over said substrate, a plurality of switching elements operationally connected to said pixel electrodes (column 1, lines 5-12 figure 1, item 12, figure 4, item 6), each of said switching elements comprising a thin film transistor (figure 1, item 12, figure 4, item 7); a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes (figure 4, item 6), and a driver circuit comprising a plurality of thin film transistors for driving said plurality of switching elements (figure 4, items 2 and 3), wherein each of the film transistors of said switching elements and said driver circuit comprises a crystalline semiconductor layer (column 3, lines 59-64), a gate insulating film adjacent to said crystalline semiconductor layer and agate electrode adjacent to said gate insulating film (figure 1, items 26, 24, and 22).

With regard to claim 20 Matsumoto teaches wherein said gate electrode is located over said semiconductor layer (figure 1, items 26 and 11) .

With regard to claim 21 Matsumoto teaches wherein all of said plurality of thin film transistors are p-type (column 5, line 67-68).

With regard to claim 22 Matsumoto teaches wherein all of said plurality of thin film transistors are n-type (column 5, line 67-68).

With regard to claim 23 Matsumoto teaches wherein said substrate is a glass substrate (column 3, line 3).

With regard to claim 24 Matsumoto teaches wherein said crystalline semiconductor layer comprises silicon (column 3, line 60).

With regard to claim 25 Matsumoto teaches In regards to claim 25 An active matrix type display device comprising: a substrate having an insulating surface, a plurality of pixel electrodes arranged in a matrix form over said substrate, a plurality of switching elements operationally connected to said pixel electrodes (column 1, lines 5-12 figure 1, item 12, figure 4, item 6), each of said switching elements comprising a thin film transistor (figure 1, item 12, figure 4, item 7), a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes (figure 4, item 6), and a driver circuit comprising a plurality of thin film transistors for driving said plurality of switching elements (figure 4, items 2 and 3), wherein each of the thin film transistors of the switching elements and the driver circuit comprises a crystalline semiconductor layer (column 3, lines 59-64), a gate insulating film adjacent to said crystalline semiconductor layer, and a gate electrode adjacent to said gate insulating film (figure 1, items 26, 24, and 22),

wherein said crystalline semiconductor layer has source and drain regions and at least one lightly doped region (column 3, lines 7-17).

With regard to claim 26 Matsumoto teaches wherein said substrate is a glass substrate (column 3, line 3).

With regard to claim 27 Matsumoto teaches wherein said source and drain regions and said at least one lightly doped region are doped with phosphorus (column 4, lines 1-35).

With regard to claim 28 Matsumoto teaches wherein said source and drain regions and said at least one lightly doped region are doped with boron (column 4, lines 1-35).

With regard to claim 29 Matsumoto teaches wherein said gate electrode is located over said semiconductor layer (figure 1, items 26 and 11) .

With regard to claim 30 Matsumoto teaches In regards to claim 30 wherein said crystalline semiconductor layer comprises silicon (column 3, line 60).

With regard to claim 31 Matsumoto teaches an active matrix type display device comprising: a substrate having an insulating surface, a plurality of pixel electrodes arranged in a matrix form over said substrate, a plurality of switching elements operationally connected to said pixel electrodes (column 1, lines 5-12 figure 1, item 12, figure 4, item 6), each of said switching elements comprising a thin film transistor (figure 1, item 12, figure 4, item 7), a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes (figure 4, item 6), and a CMOS circuit comprising at least one n-channel type thin film transistor and one p-channel type thin film transistor (column 2, line 68), wherein each of the film transistors of the switching elements and said n-channel and p-channel type thin film transistors comprises a crystalline semiconductor layer (column 3, lines 59-64), a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film (figure 1, items 26, 24, and 22).

With regard to claim 32 Matsumoto teaches wherein said substrate is a glass substrate (column 3, line 3).

With regard to claim 33 Matsumoto teaches wherein said gate electrode is located over said semiconductor layer (figure 1, items 26 and 11) .

With regard to claim 34 Matsumoto teaches wherein said crystalline semiconductor layer comprises silicon (column 3, line 60).

With regard to claim 35 Matsumoto teaches an active matrix type display device comprising: a substrate having an insulating surface, a plurality of pixel electrodes arranged in a matrix form over said substrate, a plurality of switching elements operationally connected to said pixel electrodes (column 1, lines 5-12 figure 1, item 12, figure 4, item 6), each of said switching elements comprising a thin film transistor (figure 1, item 12, figure 4, item 7), a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes (figure 4, item 6), and a CMOS circuit comprising at least one n-channel type thin film transistor and one p-channel type thin film transistor (column 2, line 68), wherein each of the film transistors of the switching elements and said n-channel and p-channel type thin film transistors comprises a crystalline semiconductor layer (column 3, lines 59-64), a gate insulating film adjacent to said crystalline semiconductor layer and a gate electrode adjacent to said gate insulating film (figure 1, items 26, 24, and 22), and said crystalline semiconductor layer has source and drain regions and at least one lightly doped region (column 3, lines 7-17).

With regard to claim 36 Matsumoto teaches wherein said substrate is a glass substrate (column 3, line 3).

With regard to claim 37 Matsumoto teaches wherein said crystalline semiconductor layer comprises silicon (column 3, line 60).

With regard to claim 38 Matsumoto teaches wherein said crystalline semiconductor layer comprises silicon (column 3, line 60).

Response to Arguments

6. Applicant's arguments filed 12/16/2002 have been fully considered but they are not persuasive.

With regard to claim 1 the 112 first new matter rejection of the phrase "a crystalline semiconductor layer", the applicant argues on pages 8-9 that "the examiner is being to restrictive with regard to this term" , the applicant gives a "general" definition of "crystalline".

The examiner disagrees with applicants position and maintains that "Amorphous Silicon" is distinctly different than Crystalline Silicon. The examiner sites two specific teaching references from the same exact field to support examiner position on this issue on how to interpret "crystalline" in the proper context of the specific field of use as actual evidence.

McCarthy (5,399,231) 3/21/1995 teaches in column 1, lines 58-63. "Due to the high temperatures of silicon processing conventional silicon-on-glass techniques have relied on amorphous (a-Si) and polycrystalline (p-Si) materials which can be doped and treated at temperatures that the glass can withstand, but whose performance is decidedly inferior to crystalline films."

McCarthy (5,414,276) 5/9/1995 teaches in column 2, lines 29-33; "In addition, a process has been recently developed to provide crystalline silicon devices on glass substrates, as described and claimed in copending application Ser. No. 08/137,411, filed Oct. 18, 1993, entitled "Crystalline Silicon Devices on Glass". "

McCarthy (5,414,276) 5/9/1995 teaches in column 2, lines 49-52; "Thus, single-crystal silicon films can be utilized, instead of the previously used amorphous and polycrystalline silicon films, in SOI devices on glass."

With regard to claims 1, 7, 13, 17, 19, 25, 31, and 35 the applicant argues on pages 9 and 10 that Matsumoto does not teach "a display medium capable of electrically changing luminous strength is for example, a light emitting material, such as an electroluminescence material"

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., is for example, a light emitting material, such as an electroluminescence material) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The examiner also disagrees because applicant is making a narrow interpretation of broad claim language "a display medium capable of electrically changing luminous strength disposed at each of said pixel electrodes" . The examiner maintains a liquid crystal display (LCD) device as taught by Matsumoto reads on this broad language. Also applicant teaches in his text and figures his apparatus being used with a liquid crystal display (LCD) device . For example on page 1 of applicant's specification;

"As a display media of such display device, a liquid crystal, plasma, an object (state) capable of electrically changing an optical characteristic (reflectance, refractive index, transmimissivity, emission (luminous) strength) or the like are used"

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Bell whose telephone number is (703) 306-3019. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Saras, can be reached at (703) 305-9720.

Any response to this action should be mailed to: Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to: (703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Paul Bell
Art unit 2675
23 January 2003

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600